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EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/531,910	YADAVALLI ET AL.
	Examiner	Art Unit
	Herng-der Day	2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Applicants' Appeal Brief ("Brief") to Office Action dated June 28, 2004, faxed September 17, 2004.

1-1. In view of the Appeal Brief, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(a) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(b) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

1-2. Claims 22, 28, and 34 have been amended. Claims 22-39 are pending.

1-3. Claims 22-39 have been examined and rejected.

Drawings

2. The proposed drawing corrections to FIG. 6 received by PTO on April 23, 2004, have been approved. The objection to the drawings has been withdrawn. When the application is allowed, Applicants will be required to submit new formal drawings.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 22-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Selvidge et al., U.S. Patent 5,649,176 issued July 15, 1997, in view of Dargelas, U.S. Patent 5, 938,785 issued August 17, 1999.

4-1. Regarding claims 22 and 24, Selvidge et al. disclose a method, comprising:

generating a netlist model for the circuit (logic netlist, column 20, lines 8-13);

providing a virtual delay element in the netlist model (flip-flop 1602 in FIG. 16B; and column 18, lines 58-63);

providing a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit (virtual clock VClk in FIG. 16B; and column 18, lines 58-65).

Selvidge et al. fail to expressly disclose generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element. Nevertheless, Selvidge et al. do disclose testing a logic design and suggest compiling and loading a netlist describing the internal architecture into a particular reconfigurable logic device and confirming that its response to inputs agrees with the design criteria (column 1, lines 30-40).

Dargelas discloses automatically determining test patterns for a netlist having multiple clocks and sequential circuits (Dargelas, Abstract). Automatic test pattern generation (ATPG) processes are used to devise test patterns using complex computer implemented processes. The

goal of ATPG processes applicable to sequential circuits is to generate test vectors to test the maximum number of stuck-at faults in the circuit (e.g., in the netlist) (Dargelas, column 1, lines 60-65). Specifically, Dargelas discloses:

(claim 1) generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element (Dargelas, Abstract);

(claim 24) the virtual clock signal is identified as a primary input of an automatic test pattern generation (ATPG) system (Dargelas, the multiple clock signals are primary input clock signals, column 6, lines 25-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Selvidge et al. to incorporate the teachings of Dargelas to obtain the invention as specified in claims 22 and 24 because Dargelas discloses automatically determining test patterns for a netlist having multiple clocks and sequential circuits to test the faults in the circuit as suggested by Selvidge et al. (column 1, lines 30-40).

4-2. Regarding claim 23, Selvidge et al. further disclose comprising:

selectively providing a virtual delay element for respective sequential element in the circuit in accordance with respective race resolution requirements of the respective sequential element (flip-flop 1602 in FIG. 16B; and column 18, lines 58-65).

4-3. Regarding claim 25, Selvidge et al. further disclose the virtual clock signal is specified by a user of the ATPG system in accordance with a physical characteristic of the circuit (Selvidge, virtual clock cycles are required for the values in the loop to settle into their final states, column 18, lines 65-67).

4-4. Regarding claim 26, Selvidge et al. further disclose the physical characteristic comprises a delay characteristic (Nested loops, column 19, lines 1-14).

4-5. Regarding claim 27, Selvidge et al. further disclose the delay characteristic corresponds to a length of conductive paths between circuit elements (cycles are nested, column 19, lines 1-14).

4-6. Regarding claims 28-33, these system claims include same method limitations as in claims 22-27 and are unpatentable using the same analysis of claims 22-27.

4-7. Regarding claims 34-39, these medium claims include same method limitations as in claims 22-27 and are unpatentable using the same analysis of claims 22-27.

Applicants' Arguments

5. Applicants argue the following:

5-1. I. The rejection of claims 22-39 under 35 U.S.C. 112, first paragraph.

(1) Claims 22, 28, and 34, "Because the language which was objected to has been deleted, the rejection of claims 22, 28, and 34 should be reversed" (page 3, Brief).

(2) Claims 25, 31, and 37, "one skilled in the art, having the benefit of the present specification, would understand how to specify the virtual clock signal in accordance with a physical characteristic of the circuit" (pages 4-5, Brief).

(3) Claims 27, 33, and 39, "one of ordinary skill in the art, having the benefit of the present specification, would understand how the delay characteristic may correspond to a length of conductive paths between circuit elements" (page 5, Brief).

5-2. II. The rejection of claims 23, 29, and 35 under U.S.C. 112, first paragraph.

(4) Claims 23, 29, and 35, "Applicants submit that the present disclosure more than adequately enables one of ordinary skill in the art to practice claims 23, 29, and 35" (page 7, Brief).

5-3. III. The rejection of claims 22-39 under 35 U.S.C. 103(a).

(5) "the Examiner's primary reference, Zeiner, is relied upon for only a single aspect of the claims, namely generating a netlist model" (page 8, last paragraph, Brief).

(6) "The Examiner suggests that the virtual element and virtual clock of Selvidge is simply the detailed implementation of the programmable delay unit in Zeiner" (page 9, third paragraph, Brief).

(7) "Selvidge discloses providing a virtual clock to a flip-flop to transform an implicit state into an explicit state. However, the cited portion is silent with respect to influencing a desired race resolution for the circuit" (page 10, first paragraph, Brief).

(8) "While Dargelas disclosed determining test patterns, the cited portion is silent with respect to other aspects of the claim recitation. Applicants have thoroughly studied the abstract of Dargelas and can find no mention of virtual delay elements or virtual clocks" (page 10, second paragraph, Brief).

(9) Claims 23, 29, and 35, "this analysis completely ignores the claim language of 'in accordance with respective race resolution requirement of the respective sequential elements'" (page 11, second paragraph, Brief).

(10) Claims 25, 31, and 37, "The cited portion is silent with respect to any physical characteristic of the circuit" (page 12, first paragraph, Brief).

(11) Claims 26, 32, and 38, "the VClk described in Selvidge is not specified in accordance with the identified delay 'period'" (page 12, third paragraph, Brief).

(12) Claims 27, 33, and 39, "The cited portion is devoid of any description related to lengths of conductive paths" (page 12, last paragraph, Brief).

Response to Arguments

6. Applicants' argument has been fully considered.

6-1. Applicants' arguments (1)-(4) are persuasive. The original claim rejections of claims 22-39 under 35 U.S.C. 112, first paragraph, have been withdrawn.

6-2. Response to Applicants' arguments (5)-(6). Under the principles of compact prosecution, the prior art of Zeiner has been introduced because Applicants amended the claims with new matter. The Examiner has indicated in the advisory action dated June 28, 2004, "Future rejections will reflect the changes to the claims entered with the proposed Amendment" and "Citing a prior art for identifying a race condition maybe not required for future art rejection". Applicants have deleted the limitation "identifying a race condition in a circuit" rendering the arguments moot because the prior art of Zeiner is not applied anymore.

6-3. Applicants' arguments (7) and (9) are not persuasive. Selvidge's invention seeks to overcome the hold time problem by imposing a new timing discipline on a given digital circuit design through a resynthesis process that yields a new but equivalent circuit (column 2, lines 43-46). Hold time violations occur when the timing signal is delayed beyond a time for which the value is valid, leading to the loss of the value (column 2, lines 15-17). In other words, Selvidge's

providing a virtual clock to a flip-flop to transform an implicit state into an explicit state is seeking to overcome the hold time problem, i.e., race resolution.

6-4. In response to Applicants' argument (8) against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In addition to disclosing virtual delay elements and virtual clocks, Selvidge et al. also suggest testing logic design which has been taught by Dargelas.

6-5. Applicants' argument (10) is not persuasive. "Additional virtual clock cycles are required for the values in the loop to settle into their final states" indicates timing requirement, which is a physical characteristic of the circuit.

6-6. Applicants' arguments (11) and (12) are not persuasive. Selvidge's invention seeks to overcome the hold time problem by imposing a new timing discipline on a given digital circuit design through a resynthesis process that yields a new but equivalent circuit (column 2, lines 43-46). If combinational cycles are nested, each can be broken by the insertion of a flip-flop and nested loops may require more clock cycles to settle (column 19, lines 10-14). In other words, nested loops and more clock cycles indicate delay characteristic associated with loops which are related to the length of conductive paths.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Jean Homere can be reached on (571) 272-3780. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day H.D.
November 29, 2004

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